

4-04-06

AF/2832/



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

---

IN RE: VINCENT, Stephen C.	)
	) APPEAL NO. _____
SERIAL NO: 10/079,010	)
	)
FOR: APPARATUS FOR TANTALUM	)
PENTOXIDE MOISTURE BARRIER	) BRIEF ON APPEAL
IN FILM RESISTORS	)
	)
FILED: February 19, 2002	)
	)
GROUP ART UNIT: 2832	)

---

To the Commissioner of Patents and Trademarks  
Mail Code Appeal Brief - Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

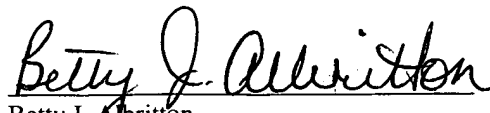
Dear Sirs:

Please enter the following Brief on Appeal into the record.

---

CERTIFICATE OF MAILING BY EXPRESS MAIL

I hereby certify that this document and the documents referred to as enclosed therein are being deposited with the U. S. Postal Service in an envelope as "Express Mail Post Office to Addressee" addressed to:  
Commissioner of Patents, Mail Code Appeal Brief - Patents, P. O. Box 1450, Alexandria, VA 22313-1450,  
prior to 5:00 p.m. on 3<sup>rd</sup> day of April, 2006.

  
Betty J. Abritton  
Express Mail Label #EV 491751419 US

## **TABLE OF CONTENTS**

I.	INTRODUCTION .....	1
II.	REAL PARTY IN INTEREST .....	1
III.	RELATED APPEALS AND INTERFERENCES .....	1
IV.	STATUS OF CLAIMS .....	2
V.	STATUS OF AMENDMENTS .....	2
VI.	SUMMARY OF CLAIMED SUBJECT MATTER .....	2
VII.	GROUND OF REJECTION TO BE REVIEWED ON APPEAL .....	3
VIII.	ARGUMENT .....	3
	A.    The § 103 Rejection of Independent Claims 7, 13, 15, 17 and 25-26 Based Upon the Combination of Yamada in View of Szupillo, Copetti or Sato is Improper.....	3
	1)    The Law of Obviousness .....	3
	2)    The Combination of the Prior Art Fails to Render Claim 7 Obvious .....	6
	3)    The Prior Art References Do Not Render Claim 13 Obvious .....	11
	4)    Claim 15 is Not Rendered Obvious By the Combination of the Prior Art References .....	11
	5)    Claim 17 is Not Rendered Obvious by the Prior Art References ..	11
	6)    Independent Claims 25 and 26 Are Not Rendered Obvious by the Prior Art References.....	12
IX.	CONCLUSION.....	14
X.	APPENDIX - Claims .....	15
XI.	EVIDENCE INDEX .....	21
XII.	RELATED PROCEEDING APPENDIX .....	22



## **I. INTRODUCTION**

This is an Appeal Brief in response to the Examiner's Final Rejection dated November 7, 2005, rejecting claims 7-10, 12, 13, 15 and 17-26. For purposes of consideration, claims 7-10, 12, and 21 are grouped together and rise and fall together. Claims 13 and 22 are grouped together and rise and fall together. Claims 15 and 23 are grouped together and rise and fall together. Claims 17-20 and 24 are grouped together and rise and fall together. Claims 25 and 26 each individually shall be considered. The claims are grouped in this manner as claims 7, 13, 15, 17, 25 and 26 are independent claims with separate basis for patentability. The appealed claims are set forth in an attached appendix.

## **II. REAL PARTY IN INTEREST**

According to MPEP § 1206, identification of the real party in interest will allow members of the Board to comply with ethic regulations. This application has been assigned to Vishay Dale Electronics, Inc., Columbus, Nebraska, Reel 012140, frame 0297 recorded September 7, 2001.

## **III. RELATED APPEALS AND INTERFERENCES**

Parent application serial number 09/829,169 is currently appealed before the United States Patent and Trademark Office Board of Patent Appeals and Interferences. No other proceeding or appeal is known to the Appellant or Appellant's legal representative or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

#### **IV. STATUS OF CLAIMS**

Claims 7-10, 12, 13, 15 and 17-26 are pending and appealed. No other claims are currently pending.

#### **V. STATUS OF AMENDMENTS**

All amendments have been entered.

#### **VI. SUMMARY OF CLAIMED SUBJECT MATTER**

The present invention relates to method and apparatus for a thin film chip resistor having a tantalum pentoxide moisture barrier (see Specification, page 1, first paragraph under the section titled Background of the Invention).

Any thin film resistors, especially those of nickel-chromium alloys and other alloys containing nickel, chromium or other metals are particularly susceptible to moisture conditions (see Specification, page 1, lines 31-34). This susceptibility to moisture can lead to failure of the resistive element if the resistor is used in moist conditions. In particular, under powered moisture conditions, electrolytic corrosion can occur and a resistor can fail. This makes the thin film resistor unsuitable for applications where moisture conditions may occur (see Specification, page 2, lines 2-6).

Tantalum pentoxide has been used in the semiconductor industry as a dielectric but not as a moisture barrier. Tantalum nitride resistors have been used in the resistor industry to prevent moisture failures (see Specification, page 1, lines 24-30). It is recognized that tantalum nitride resistors have a naturally occurring layer of tantalum pentoxide as a result of the natural oxidation process. This natural oxidation process provides moisture resistance,

but does not provide a sufficient moisture barrier to use thin film resistors in powered moisture environments, and restricts the composition of the resistor to one with tantalum nitride resistor elements.

The present invention promotes any number of metal films to be used as a resistive element. In particular, the invention permits nickel-chromium alloys to be used in situations that a moist condition might occur (see Specification, page 3, lines 20-24). In the present invention the metal film layer is overlaid with a moisture barrier of tantalum pentoxide that acts as a moisture barrier and prevents electrolytic corrosion that causes electrical open conditions under certain moisture conditions (see Specification, page 3, lines 28-32).

## **VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

Claims 7-10, 12-13, 15, and 17-26 have been rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent No. 6,023,217 to Yamada et al. in view of U.S. Patent No. 3,474,305 to Szupillo, U.S. Application No. 2001/0017770 to Copetti et al. or Sato (61-27264). Each of these rejections is presented for review on appeal.

## **VIII. ARGUMENT**

### **A. The § 103 Rejection of Independent Claims 7, 13, 15, 17 and 25-26 Based Upon the Combination of Yamada in View of Szupillo, Copetti or Sato is Improper.**

#### **1) The Law of Obviousness**

"A claimed invention is unpatentable if the difference between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the pertinent art." In re Kahn, 04-1616, 2006 W.L. 708687, at \*10 (Fed. Cir. 2006). "Most inventions arise from a combination of old elements and each element may often be found in the prior art." Id. at \*11. "However, mere identification in the prior art of each element is insufficient to defeat the patentability of the combined subject matter as a whole." Id. "Rather, to establish a *prima facie* case of obviousness based on a combination of elements disclosed in the prior art, the Board must articulate the basis on which it concludes that it would have been obvious to make the claimed invention." Id.

"In practice, this requires that the Board explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." Id. The Federal Circuit explained that the inquiry into whether a skilled artisan would have been motivated to combine references is meant to defend against the insidious effect of hindsight. The proper test to prevent hindsight and using the current application as a road map is the "motivation-suggestion-teaching" test. This "test asks not merely what the references disclose, but whether a person of ordinary skill in the art, possess with the understanding and knowledge reflected in the prior art, and motivated by the general problem facing the inventor, would have been led to make the combination recited in the claims." Id. at \*16.

The Federal Circuit has further elaborated that "under § 103, teachings of references can be combined under only if there is some suggestion or incentives to do so . . . the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the

modification." (*emphasis added*). In re Fritch, 972 F.2d 1260, 1266 (Fed. Cir. 1992). More particularly, the Federal Circuit has stated that for a § 103 obviousness rejection based on a combination of patents, there must be some objective teaching leading to the combination. See Id. at 1265. As further explained by the Federal Circuit at In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999), this showing must be "clear and particular".

The Examiner has failed to meet this requisite burden in the current application. The Examiner's limited statement regarding proposed motivation to combine is "that one known prior art dielectric can be replaced for another since they are both dielectric and are used as barriers, and are compatible with the same materials." This overly simplistic statement fails to meet the burden outlined at In re Kahn that "rejections on obviousness grounds cannot be sustained by mere conclusory statements, [but] instead, there must be some articulated reasoning that some rational underpinning to support the legal conclusion of obviousness." In re Kahn, at \*15. The analysis is further logically flawed in that not all prior art dielectric are equal when being used as a moisture barrier for a thin film resistor, and that all dielectric barriers are not moisture barriers. For reasons outlined below, the combination of the prior art references fail to provide the necessary motivation or suggestion to combine and render the current application obvious.

Additionally, Applicant's specific use of tantalum pentoxide as a moisture barrier in a thin film resistor is not disclosed or taught in Yamada, Sato, Copetti or Szupillo. In fact, none of the cited references teach that tantalum pentoxide can be used as a moisture barrier. Sato is directed to a thermal head and not a thin film chip resistor and discloses sputtering a layer of tantalum pentoxide as an abrasive resistance layer. Copetti uses dielectric such as

tantalum pentoxide as an insulator layer to separate conductive layers. Szupillo discloses using oxide film to form an electrical insulative barrier layer. Thus, it would be obvious to use tantalum oxide as an abrasive resistant insulative and electrically insulative layer, but not as a moisture resistant layer. The cited references simply do not teach that tantalum oxide has a very low moisture uptake, thus providing a moisture resistant layer when used as a barrier, as Applicant has done.

**2) The Combination of the Prior Art Fails to Render Claim 7 Obvious.**

Not all dielectrics are equal for each and every application. The Examiner suggests this very ideal when the Examiner states that "one known prior art dielectric can be replaced for another since they are both dielectrics and are used as barriers, and are compatible with the same materials." This motivation is fatally flawed. Anyone who has walked in the rain knows that air, a known dielectric, does not provide a moisture barrier. Thus, just because two materials are both dielectrics and thus serve as electrical barriers does not mean they would be expected to provide the same barrier to moisture. Of course, there are many other examples of dielectrics that are hydrophilic, that is those having a high moisture uptake, that is used because it can form a barrier and is compatible with nichrome. A specific example of a dielectric barrier that is hydrophilic and compatible with nichrome or polyamides. Yet, replacing the screen from the layer of Yamada with certain polyamides ("one known prior art dielectric"), as suggested by the Examiner, totally defeats Applicant's objectives and teaches directly away from independent claim 7, 13, 15, 17 and 25-26, which requires a thin chip resistor resistant to moisture or electrolytic corrosion. Attached as Exhibit 1 on page 43 is

further evidence that dielectrics that form barriers that do not necessarily form moisture barriers.

Claim 7 would not be obvious over Yamada in view of Szupillo, Copetti, or Sato. Claim 7 requires a thin film chip resistor "without use of a screen printed moisture barrier." Yamada discloses an outer protective barrier 24 which is a thermally cured and screen printed resin paste (column 3, lines 40-41 and column 4, lines 18-22). Alternatively, Yamada discloses screen printing a protective layer 54 with glass paste (column 17, lines 65-column 8, line 3). This teaching is contrary to the claimed invention. Moreover, a primary objective of the Applicant's invention is to provide "a moisture barrier for a thin film resistor [which] replaces screen printed moisture barriers." (Specification, page 2). It is a further objective of the present invention to provide for a "moisture barrier for a thin film resistor that is compatible with normal manufacturing techniques and materials" (Specification, page 2). The screen-printed moisture barriers used by Yamada is contrary to the "formed from deposition" limitation and "without use of a screen-printed moisture barrier" limitation. Thus, Yamada is wholly inconsistent with both of Applicant's objectives and the claim language. Claim 7 further requires "an outer moisture barrier formed from deposition of tantalum oxide on the metal thin film resistive layer and not through oxidation of tantalum." Yamada discloses no such teaching and the Examiner concurs (Office Action, page 2, numbered paragraph 2). These limitations emphasize the difference between Yamada and the claimed invention.

Applicant's work recognizes problems in the prior art that Yamada does not address. Whereas Applicant's invention provides a moisture barrier to a non-tantalum thin film

resistor without screen-printing, Yamada's invention does not. Here, neither Yamada nor the other prior art references, speak to the particular problem addressed by the present invention and the problem that is clearly presented in the claims. Specifically, claim 7 requires the barrier be addressed by creating a moisture barrier "without use of a screen-printed moisture barrier." In short, as stated by the Federal Circuit, "the problem solved by the invention is always relevant." In re Wright, 838 F.2d 1216, 6 U.S.P.Q.2d 1959, 1961 (Fed. Cir. 1988).

Claim 7 is not obvious in view of combining Yamada and Szupillo. For instance, claim 7 requires "a continuous metal thin film resistive layer." Szupillo does not disclose the continuous thin film layer of Applicant's claimed invention. Instead, Szupillo is specifically directed towards a discontinuous layer of film. Szupillo further discloses oxidizing tantalum film to produce tantalum pentoxide (col. 8, lines 5-21). Thus, Szupillo cannot fairly be used to disclose using both a non-tantalum thin film and a layer of tantalum pentoxide in the same device. Moreover, Szupillo's use of tantalum oxide is for a different purpose than Applicants. Furthermore, the deposition of tantalum pentoxide in Szupillo does not serve as an outer moisture barrier as required by claim 7, but rather serves as an insulator. This is clear from column 5, lines 23-27 which refers to a barrier layer 22 as "composed of a suitable electrical insulating material such as silicone dioxide, barium oxide, tantalum pentoxide, titanium dioxide or the like." Thus, Szupillo makes clear that there is an electrical insulating layer but does not treat or use this electrical insulating layer as a moisture barrier. Therefore, it is respectfully submitted that the Examiner has not established a *prima facie* case of obviousness in respect to this combination as there would be no teaching or motivation to use tantalum pentoxide as the moisture barrier based on these two prior art references.

Claim 7 is also not obvious in view of combining Yamada and Copetti. In particular, it is observed that Copetti teaches a module that includes a thin-film circuit. In Copetti, capacitors, or capacitors and resistors, or capacitors, resistors and inductors are provided next to the conductive track directly on a substrate of an insulating material (Abstract). Each of the disclosed embodiments of Copetti requires both a dielectric layer and protective layer. Further yet, each embodiment requires "at least one contact hole passing through the module" (col. 3, line 29). Having a contact hole through both the dielectric and protective layer to facilitate creation of electrical conduit between barriers would not form an effective moisture barrier as required by claim 7. Thus, Copetti teaches away from Applicant's claimed invention.

Copetti discloses using tantalum pentoxide is one of a number of dielectrics because of its relative dielectric constant (col. 2, lines 60-68). Copetti does not select a tantalum pentoxide for use as a moisture barrier, but simply as a dielectric. Furthermore, Copetti uses a separate protective layer to protect the adjacent layers from a chemical load and corrosion by moisture (col. 3, lines 1-4), thereby indicating that Copetti does not foresee using tantalum pentoxide as a moisture barrier. Thus, Copetti actually teaches away from the use of the tantalum pentoxide as a moisture barrier as Copetti uses a separate moisture barrier, and hence Copetti can provide no proper motivation to combine with the other cited reference to provide a moisture barrier.

Claim 7 is also not obvious in view of combining Yamada and Sato. In the Examiner's combination of Yamada with Sato, the Examiner indicates that "Sato discloses sputtering a tantalum pentoxide layer for the purpose of providing a protective layer so that it

would have been obvious to employ a sputtered layer, to replace a protective layer of Yamada, for protection where the references disclose a protection layer or double protection layer for a resistor." (Office Action, 7-14-2005, page 2, numbered paragraph 2). To the extent the Examiner relies upon Sato, it is noted that Sato is directed towards a very different type of an invention, namely a thermal head. Just because a thermal head includes heat-generating resistors is not enough to make a thermal head an analogous art. In relying upon Sato, the Examiner fails to acknowledge that a thermal head is not a chip resistor. Moreover, the purpose of the abrasion resistant layer 6 in Sato is to stabilize printing quality by forming a protective layer before applying the heat treatment. The Examiner does not use Sato for this purpose. In addition, the Examiner does not properly consider the differences and purposes for using a protective layer in the context of a thermal head and a protective layer in the context of a thin filmed strip resistor.

The Examiner's consideration of the layer only as "protection" is too general and not specific enough to establish a proper rejection, particularly in light of the recent Federal Circuit decision In re Kahn. It is respectfully submitted that the Examiner did not make a *prima facie* case of obviousness as the Examiner has not provided a proper motivation or suggestion to combine these references. It is further observed that the Examiner has not specifically cited to either reference for the proposition that a sputtered tantalum oxide layer of a thermal head in Sato should replace a cured epoxy resin or glass protective layer of a chip resistor of Yamada. Instead, the Examiner relies upon hindsight reconstruction that eviscerate, that which makes the invention patentable or using tantalum pentoxide as an outer moisture barrier in a chip resistor.

As claims 8-10, 12 and 21 depend from claim 7, it is respectfully submitted that these rejections be reversed as well.

**3) The Prior Art References Do Not Render Claim 13 Obvious.**

For all the reasons stated above, Yamada in view of Sato, Szupillo or Copetti does not render claim 13 obvious. Further, there is an independent basis for patentability for claim 13. Claim 13 requires "a moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the nickel-chromium alloy thin film layer for reducing failures due to electrolytic corrosion under powered moisture conditions." Neither Yamada nor Copetti discloses this limitation. At best, Copetti discloses use of tantalum pentoxide as an insulator and discloses an outer moisture barrier of a different material. Thus, neither reference discloses using tantalum pentoxide as a moisture barrier in a resistor. Therefore this rejection should also be reversed.

**4) Claim 15 is Not Rendered Obvious By the Combination of the Prior Art References.**

With respect to claim 15 an independent basis for patentability exists. Claim 15 requires "an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the passivation layer for reducing failures due to electrolytic corrosion under powered moisture conditions" and "the outer moisture barrier formed from deposition of tantalum oxide on the passivation layer". These limitations are not disclosed in neither Yamada nor Copetti, therefore, this rejection should be reversed.

**5) Claim 17 is Not Rendered Obvious by the Prior Art References.**

Claim 17 includes the limitations that "a thin film chip resistor resistant to failures due to electrolytic corrosion under powered moisture conditions without use of tantalum

nitride system and without use of screen printed moisture barriers" and "an outer moisture barrier consists of tantalum pentoxide directly overlaying and contacting the thin film resistive element to reduce failure due to electrolytic corrosion under powered moisture conditions." These limitations are not disclosed in neither Yamada nor Copetti. Therefore, this rejection should be reversed.

**6) Independent Claims 25 and 26 Are Not Rendered Obvious by the Prior Art References.**

Claims 25 and 26 distinguish over the prior art references by providing specific product by process limitations. The product by process claims for manufacturing the thin film chip resistors renders the product distinct since there are structural distinctions created by the process. Specifically, the structure in Yamada does not disclose an outer layer of tantalum oxide overlaying the metal film resistive layer, as required by the new claims. Applicant's claimed invention is not a thermal head like Sato and thus has structural differences over Sato. In Sato, the resistance heating element is coated with a low melting point glass which comes in contact with recording paper to prevent oxidation of the thermal head. Whereas, in Applicant's invention, a metal film resistant layer is overlaying the resistor substrate. Additionally, Sato does not contemplate nor consider using sputtered layer of tantalum pentoxide as a moisture barrier. Copetti calls for using dielectrics such as tantalum pentoxide as an insulator layer to separate conductive layers, in addition to at least one contact hole, which passes through the module. Applicant's use of tantalum pentoxide is to eliminate moisture uptake by the thin film chip resistor and is overlaying the resistor substrate. Szupillo discloses that the second and outer barrier layer 26 is barium oxide, not tantalum pentoxide. Applicant's barrier is tantalum pentoxide. Furthermore, Szupillo uses

eliminate moisture uptake by the thin film chip resistor and is overlaying the resistor substrate. Szupillo discloses that the second and outer barrier layer 26 is barium oxide, not tantalum pentoxide. Applicant's barrier is tantalum pentoxide. Furthermore, Szupillo uses oxidized film to form an electrically insulative barrier layer, yet Applicant's tantalum pentoxide is not formed by natural oxidation.

In addition, there are additional secondary indicia of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1 (1966). For example Applicant has obtained substantially similar claims to those of claim 25 and 26 in related case EP 1377990 (Exhibit 2). The fact that such claims have been found to provide inventive step under European Patent Laws is further evidence of non-obviousness and thus should be considered as a secondary indicia of non-obviousness.

## **IX. CONCLUSION**

The combinations of Yamada with Szupillo, Copetti or Sato cannot support an obviousness rejection under § 103. The Examiner's rejections must be reversed and the case allowed.

Enclosed herein please find the Appeal Brief and required fee of \$500.00. If this amount is not correct, please consider this a request to debit or credit Deposit Account No.

26-0084 accordingly.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "John D. Goodhue", written over a horizontal line.

JOHN D. GOODHUE, Reg. No. 47,603  
McKEE, VOORHEES & SEASE  
801 Grand Avenue, Suite 3200  
Des Moines, Iowa 50309-2721  
Phone No. (515) 288-3667  
Fax No. (515) 288-1338  
**CUSTOMER NO: 22885**  
Attorneys of Record

JFL/bja-pw

**X. APPENDIX - CLAIMS**

1-6 (Canceled).

7. A thin film chip resistor resistant to moisture without use of metallic tantalum and without use of a screen-printed moisture barrier comprising:  
a substrate;  
a single continuous metal thin film resistive layer directly attached to the substrate, the metal thin film layer being non-tantalum;  
a non-tantalum chip resistor termination attached on each end of the metal thin film resistive layer;  
an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the metal thin film resistive layer for reducing failures due to electrolytic corrosion under powered moisture conditions; and  
the outer moisture barrier formed from deposition of tantalum oxide on the metal thin film resistive layer and not through oxidation of tantalum.

8. The thin film resistor of claim 7 wherein the metal film layer is an alloy containing nickel.

9. The thin film resistor of claim 7 wherein the metal film layer is an alloy containing chromium.

10. The thin film resistor of claim 7 wherein the metal film layer is a nickel-chromium alloy.

11. (Canceled).

12. The thin film resistor of claim 7 wherein the tantalum pentoxide layer is overlaid by sputtering.

13. A nickel-chromium alloy thin film chip resistor resistant to moisture without use of metallic tantalum and without use of a screen-printed moisture barrier comprising:  
an alumina substrate;  
a single nickel-chromium alloy thin film layer directly contacting the substrate;  
a non-tantalum chip resistor termination attached on each end of the nickel-chromium alloy thin film;  
an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the nickel-chromium alloy thin film layer for reducing failures due to electrolytic corrosion under powered moisture conditions; and  
the outer moisture barrier formed from deposition of tantalum oxide on the nickel-chromium alloy thin film layer and not through oxidation of tantalum.

14 (Canceled).

15. A nickel-chromium alloy thin film chip resistor resistant to moisture without use of metallic tantalum and without use of a screen-printed moisture barrier comprising:  
an alumina substrate;  
a single nickel-chromium alloy thin film layer directly contacting the substrate;  
a non-tantalum chip resistor termination attached on each end of the nickel-chromium alloy thin film;  
a passivation layer directly overlaying and contacting the nickel-chromium alloy layer;  
an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the passivation layer for reducing failures due to electrolytic corrosion under powered moisture conditions; and  
the outer moisture barrier formed from deposition of tantalum oxide on the passivation layer and not through oxidation of tantalum.

Claim 16 (Canceled).

17. A thin film chip resistor resistant to failures due to electrolytic corrosion under powered moisture conditions without use of a tantalum nitride system and without use of a screen-printed moisture barrier, comprising:

a substrate;

a single thin film resistive element overlaid on the substrate;

a chip resistor termination attached on each end of the thin film resistive element; and

an outer moisture barrier consisting of tantalum pentoxide directly overlaying and contacting the thin film resistive element to reduce failures due to electrolytic corrosion under powered moisture conditions.

18. The thin film chip resistor of claim 17 wherein the outer moisture barrier prevents failure after MIL-STD-202 testing.

19. The thin film chip resistor of claim 17 wherein the chip resistor termination is wrap around termination.

20. The thin film chip resistor of claim 17 wherein the thin film resistive element is a metal thin film resistive element.

21. The thin film chip resistor of claim 7 manufactured by: depositing the metal film resistive layer directly overlaying and attaching to the thin film chip resistor substrate; attaching the chip resistor termination on each end of the metal film resistive layer; and depositing the moisture barrier consisting essentially of a layer of tantalum pentoxide film overlaying the metal film resistive layer to reduce failures due to electrolytic corrosion under powered moisture conditions, the layer of tantalum pentoxide not being formed by natural oxidation of the metal thin film resistive layer.

22. The nickel-chromium alloy thin film chip resistor of claim 13 manufactured by: depositing the alloy thin film layer directly contacting the alumina substrate; attaching the chip resistor termination on each end of the alloy thin film layer; and depositing the moisture barrier consisting essentially of a layer of tantalum pentoxide film directly overlaying and contacting the alloy thin film layer to reduce failures due to electrolytic corrosion under powered moisture conditions, the layer of tantalum pentoxide not being formed by natural oxidation of the alloy thin film layer.

23. The nickel-chromium alloy thin film chip resistor of claim 15 manufactured by: depositing the alloy thin film layer directly contacting the alumina substrate; attaching the chip resistor termination on each end of the alloy thin film layer; depositing the passivation layer directly overlaying the alloy thin film layer; and depositing the moisture barrier consisting essentially of a layer of tantalum pentoxide film directly overlaying and contacting the passivation layer to reduce failures due to electrolytic corrosion under powered moisture conditions, the tantalum pentoxide layer not being formed naturally by oxidation.

24. The thin film chip resistor of claim 17 manufactured by: overlaying the resistive element on the substrate; attaching the chip resistor termination on each end of the thin film resistive element; and depositing the moisture barrier consisting essentially of a layer of tantalum pentoxide film overlaying the resistive element to reduce failures due to electrolytic corrosion under powered moisture conditions, the layer of tantalum pentoxide not being formed by natural oxidation of the resistive element.

25. A thin film chip resistor, comprising:  
a substrate;  
a metal thin film resistive layer directly attached to the substrate;  
a chip resistor termination attached on each end of the metal thin film resistive layer; and

an outer moisture barrier consisting essentially of tantalum pentoxide directly overlaying and attaching to the metal thin film resistive layer for reducing failures due to electrolytic corrosion under powered moisture conditions, the tantalum pentoxide not being formed by natural oxidation of the metal thin film resistive layer; wherein the thin film chip resistor is manufactured by:

- (a) depositing a metal film resistive layer directly overlaying and attaching to a thin film chip resistor substrate;
- (b) attaching a chip resistor termination on each end of the metal film resistive layer; and
- (c) depositing the moisture barrier consisting essentially of a layer of moisture barrier consisting essentially of a layer of tantalum pentoxide film overlaying the metal film resistive layer to reduce failures due to electrolytic corrosion under powered moisture conditions, the layer of tantalum pentoxide not being formed by natural oxidation of the metal thin film resistive layer.

26. A thin film chip resistor, comprising:

a resistive substrate;

a metal thin film resistive layer directly attached to the substrate, the metal thin film being non-tantalum;

a chip resistor termination attached on each end of the metal thin film resistive layer;

a passivation layer directly overlaying the metal-thin film resistive layer;

an outer moisture barrier consisting of tantalum pentoxide directly overlaying the passivation layer for reducing failures due to electrolytic corrosion under powered moisture conditions, the tantalum pentoxide layer not being formed naturally by oxidation wherein the thin film chip resistor is manufactured by:

- (a) depositing the metal film resistive layer directly overlaying and attaching to the thin film chip resistor substrate;
- (b) attaching the chip resistor termination on each end of the metal film resistive layer;

- (c) depositing a passivation layer directly overlaying the metal-thin film resistive layer; and
- (d) depositing the moisture barrier consisting essentially of a layer of tantalum pentoxide film overlaying the passivation layer to reduce failures due to electrolytic corrosion under powered moisture conditions, the layer of tantalum pentoxide layer not being formed naturally by oxidation.

**XI. EVIDENCE APPENDIX**

Attached at Exhibit 1 on page 43 is further evidence that dielectrics that form barriers do not necessarily form moisture barriers.

Attached at Exhibit 1 is a copy of EP 1377990, which is directed toward the same invention.

**XII. RELATED PROCEEDING APPENDIX**

No decisions have been rendered by a court or the Board in any proceeding identified under Section III of the current appeal brief.

**PROCESS INTEGRATION ISSUES  
OF LOW-PERMITTIVITY DIELECTRICS  
WITH COPPER FOR HIGH-PERFORMANCE  
INTERCONNECTS**

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

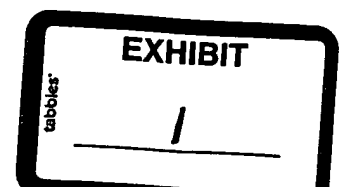
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF Ph.D.

CHAPTER 3

Alvin Leng Sun Loke

March 1999



## **Chapter 3 Low-Permittivity Dielectrics**

---

Interlevel dielectrics (ILD's) currently incorporated in IC manufacturing are deposited oxides with dielectric constants ( $\kappa$ 's) ranging from 4.0 to 4.5. As explained in Chapter 1, substituting the oxide ILD's with lower  $\kappa$  materials improves the performance of interconnects through reduction of parasitic capacitance. Capacitance reduction mitigates crosstalk noise, dynamic power dissipation, and interconnect propagation delay issues as interconnects continue to scale.

This chapter focusses on the chemistry and materials aspects of low-permittivity (low- $\kappa$ ) dielectrics, starting with a brief discussion of the physical properties that make a dielectric low- $\kappa$ . A survey of materials that are developed as prospective future ILD materials is then presented. Emphasis is placed on the six low- $\kappa$  polymer dielectrics that are studied in this dissertation.

### **3.1 Strategies for Dielectric Constant Reduction**

The dielectric constant,  $\kappa$ , is a physical measure of the electric polarizability of a material [68]. Electric polarizability is the tendency of a material to allow an externally applied electric field to induce electric dipoles (separated positive and negative charges) in the material. Shown in Eq. (3-1),  $\kappa$  can be expressed as

### Chapter 3: Low-Permittivity Dielectrics

$$\kappa = \frac{\epsilon}{\epsilon_0} = \frac{\epsilon_0(1 + \chi_e)}{\epsilon_0} = 1 + \chi_e \quad (3-1)$$

where  $\epsilon$  and  $\epsilon_0$  are the permittivities of the dielectric and free space respectively, and  $\chi_e$  is the electric susceptibility of the dielectric.  $\chi_e$  is the unitless constant of proportionality relating the induced dipole moment per unit volume of dielectric,  $\vec{P}$ , to the applied electric field,  $\vec{E}$ .

$$\vec{P} = \epsilon_0 \chi_e \vec{E} \quad (3-2)$$

In a perfect vacuum, there are no atoms to polarize, making  $\chi_e = 0$  and  $\kappa = 1$ . In solid-state matter, there are three polarization mechanisms: electronic, atomic, and dipolar [69]. Electronic polarization occurs in neutral atoms when an electric field displaces the nucleus with respect to the electrons that surround it. Atomic polarization occurs when adjacent positive and negative ions stretch under an applied electric field. Dipolar or orientational polarization occurs when permanent dipoles in asymmetric molecules respond to the applied electric field. Each polarization mechanism has an associated response time and therefore will not contribute to  $\kappa$  beyond some corresponding frequency. Figure 3-1 illustrates a typical  $\kappa$  dependence on the frequency of the applied field. All three mechanisms respond to GHz or lower frequencies where IC's operate.

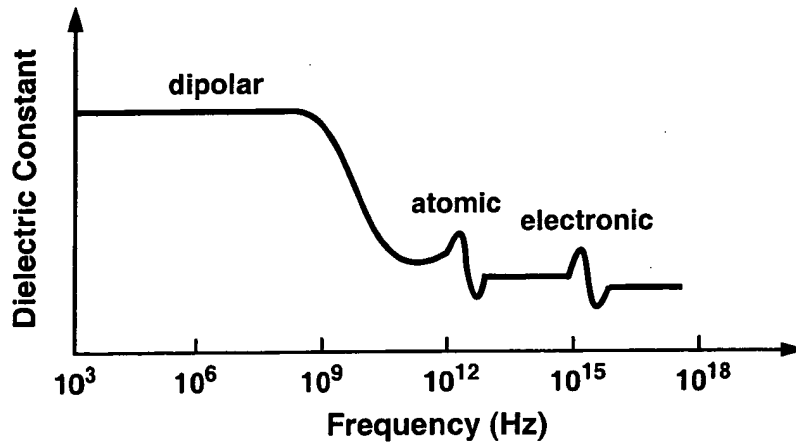


Figure 3-1 Frequency response of dielectric mechanisms [69].

### 3.2 Survey of Available Materials

A low- $\kappa$  dielectric is an insulating material that exhibits weak polarization when subjected to an externally applied electric field. There are many guidelines employed to design low- $\kappa$  materials. A few practical approaches are briefly mentioned. The most obvious one is to choose a nonpolar dielectric system. For example, polarity is weak in materials with few polar chemical groups and with symmetry to cancel the dipoles of chemical bonds between dissimilar atoms. Since  $\kappa_{air} \approx 1$ , dielectrics can also have lower effective  $\kappa$ 's with the incorporation of some porosity into the chemical structure. Another approach is to minimize the moisture content in the dielectric or alternatively design a dielectric with minimum hydrophilicity. Since  $\kappa_{water} \approx 80$ , a low- $\kappa$  dielectric needs to absorb only very small traces of water before losing its permittivity advantage.

### 3.2 Survey of Available Materials

Strictly speaking, air has the lowest  $\kappa$ , exhibiting more than 75% permittivity improvement over conventional oxide ILD's. Unfortunately, many reliability concerns exist with the implementation of air as the ILD, the obvious one being the structural integrity of the interconnects. Some of these issues can be mitigated by deliberately integrating air voids, for example, using an unconformal oxide deposition during gapfill [70]. However, the manufacturability of these approaches remain to be demonstrated. For a low- $\kappa$

**Table 3-1: Property Requirements of Low- $\kappa$  Dielectrics**

Electrical	Chemical	Mechanical	Thermal
Dielectric constant Anisotropy Low dissipation Low leakage current Low charge trapping High electric-field strength High reliability	Chemical resistance Etch selectivity Low moisture uptake Low solubility in H <sub>2</sub> O Low gas permeability High purity No metal corrosion Long storage life Environmentally safe	Thickness uniformity Good adhesion Low stress High hardness Low shrinkage Crack resistance High tensile modulus	High thermal stability Low coefficient of thermal expansion Low thermal shrinkage Low thermal weight loss High thermal conductivity

### Chapter 3: Low-Permittivity Dielectrics

---

dielectric to be considered suitable for backend integration, it must satisfy a multitude of electrical, chemical, mechanical, and thermal requirements summarized in Table 3-1. These requirements invariably introduce compromises which must be carefully considered in order to engineer feasible low- $\kappa$  materials for the ILD application.

The families of dielectric materials currently available for ILD integration are listed in Table 3-2. These dielectrics are deposited on the wafer either by CVD or by spin-on deposition. CVD offers the advantages of being a dry process, capable of producing films with excellent uniformity and conformality [71]. However, CVD is generally restricted to dielectrics with relatively simple chemistries. A larger variety of materials can be deposited by spin-on deposition [72], much like photoresist. Dissolved in a solvent, spin-on low- $\kappa$  precursors are first dispensed onto the wafer in liquid form. The coating is subsequently cured to expel the solvent and induce polymerization and crosslinking of the precursors in order to form a solvent-resistant dielectric with desirable electrical, mechanical, chemical, and thermal properties.

Fluorinated oxide shares many integration similarities as undoped plasma oxides and is extensively developed as the next generation ILD with  $\kappa = 3.5$  [21]. Fluorinating a

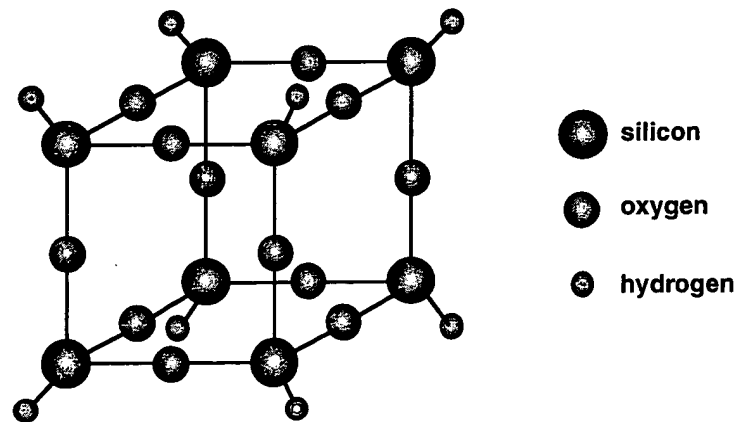
**Table 3-2: Families of Candidate Low- $\kappa$  Dielectrics for Advanced Interconnects**

Dielectric Materials	$\kappa$	Deposition Method
undoped plasma $\text{SiO}_2$	4.0–4.5	CVD
fluorinated $\text{SiO}_2$	3.5	CVD
spin-on glasses (silsesquioxanes)	2.2–3.0	spin-on
organic polymers (e.g., polyimides, parylenes, aromatic ethers)	2.0–3.9	spin-on / CVD
fluorinated amorphous carbon ( $\alpha\text{-C:F}$ )	2.1–2.3	CVD
nanoporous dielectrics (e.g., xerogels)	1.2–2.2	spin-on

dielectric is a common means of reducing  $\kappa$  provided that the fluorine atoms are incorporated correctly. Fluorine is the most electronegative atom and forms chemical bonds that are not easily perturbed by external electric fields and hence not readily polarizable. However, since fluorine is also highly reactive, excessive fluorination raises concerns of metal and dielectric corrosion. Even though  $\kappa$  as low as 3.2 can be attained, excessive fluorination of oxide additionally introduces moisture uptake and thermal stability issues.

Below  $\kappa$  of 3.5, spin-on glasses (SOG's) have been actively investigated and are already used in production [35]. Before CMP was introduced in manufacturing, SOG's were considered primarily because of their ability to planarize the topography of Al lines and spaces for multilevel integration. Common SOG's are hydrogen silsesquioxane (HSQ) and methyl silsesquioxane (MSQ). Silsesquioxanes or siloxane-based dielectrics are caged silica structures, shown in Figure 3-2, which enclose empty pores for low  $\kappa$ . They are thermodynamically unstable and upon heating at 450°C or beyond, will transform into more densified amorphous  $\text{SiO}_2$ , thereby losing its permittivity advantage [72].

Organic polymers have also received significant consideration as ILD materials. Polyimides were first considered because they possess good mechanical strength, thermal stability, and chemical resistance [73] as well as have an established usage in printed cir-



**Figure 3-2** Structural formula of a hydrogen silsesquioxane spin-on glass.

### Chapter 3: Low-Permittivity Dielectrics

---

cuit board manufacturing. However, with  $\kappa$  values typically exceeding 3.0, polyimides cannot meet future ILD requirements. Moreover, polyimides readily absorb ambient moisture and exhibit significant anisotropy in the dielectric constant. The polyimide system can be modified to mitigate these limitations, but the improvements are only incremental. These shortcomings have stimulated the chemical industry to develop completely different families of low- $\kappa$  polymer dielectrics specifically tailored for ILD integration. Some of the spin-on varieties include polyarylene ethers, derivatives of cyclobutane, polynorbornenes, amorphous Teflon™, and phase-separated inorganic-organic hybrids. CVD alternatives include parylene-N, parylene-F, polynaphthalene, and polytetrafluoroethylene (Teflon™). Some of these materials will be further discussed in Section 3.3.

Other dielectrics receiving recent attention include diamond-like carbon [74] and fluorinated amorphous carbon [75]. These materials are attractive primarily because they are deposited by CVD using existing tools. Diamond-like carbon exhibits thermal stability and adhesion issues although it has been successfully incorporated in a single-Damascene demonstration [74].  $\kappa$  can be reduced to as low as 2.1 by introducing fluorine although fluorination further degrades thermal stability and adhesion.

Nanoporous dielectrics are among the few materials options with ultralow  $\kappa$  ( $< 2.0$ ). They include xerogels, aerogels, and organic nanofoams [76]. To date, the most active integration effort is with xerogel, a spin-on porous silica matrix. Unlike the previously described families of low- $\kappa$  dielectrics,  $\kappa$  of xerogel is tunable depending on the degree of porosity that is incorporated during processing. Process integration of porous materials is very challenging because these dielectrics are mechanically weak and have large internal surface areas which can absorb moisture. The pores also degrade dielectric breakdown strength as well as increase the difficulty of depositing continuous films on these dielectric surfaces. Nevertheless, Damascene Cu integration with oxide-encapsulated xerogel has been demonstrated [33]. The potentially significant capacitance advantage of xerogel remains to be shown.

### 3.3 Investigated Dielectrics

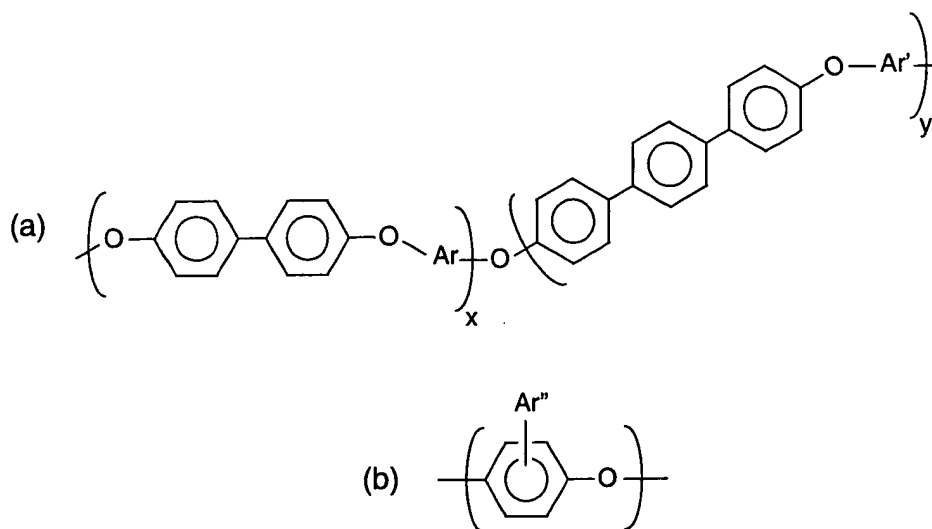
Six low- $\kappa$  organic polymer dielectrics were studied in this dissertation. As listed in Table 3-3, they consist of five spin-on polymers and one CVD polymer. The chemistries of these materials share some similarities which are incorporated to meet the ILD integration requirements. In designing carbon-based low- $\kappa$  materials, the most challenging requirement to meet is thermal stability. At temperatures of 400–450°C and beyond, the polymer network begins to disintegrate as there is sufficient thermal energy to break chemical bonds. Thermal stability is improved in polymers which are highly crosslinked and have rigid backbones, aromatic structures, and highly polar groups. Crosslinking additionally increases mechanical strength and solvent resistance. However, aromaticity and polarity increase both  $\kappa$  and water absorption.

**Table 3-3: Investigated Low- $\kappa$  Dielectrics**

Low- $\kappa$ Polymer Family	Specific Variety	$\kappa$
polyarylene ether	Schumacher PAE-2 [77]	2.8
	Asahi Chemical ALCAP-E [78]	2.8
aromatic hydrocarbon	Dow Chemical SiLK™ polymer [79]	2.7
fluorinated polyimide	DuPont FPI-136M [82]	2.6
benzocyclobutene	Dow Chemical Cyclotene™ 5021 BCB [83]	2.6
polyarylene-F	Novellus Systems AF-4 [85]	2.4

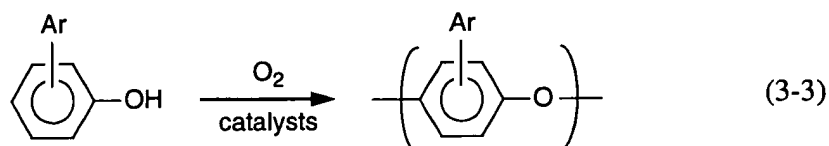
#### 3.3.1 Polyarylene Ether

Polyarylene ethers consist of aromatic groups (Ar) connected by ether oxygen linkages in a linear fashion. Compared to other functional groups (e.g., carboxylic acids, aldehydes, esters, and ketones), ether linkages provide strong C–O bonds for improved thermal stability while introducing relatively weak polarity for low  $\kappa$ . Two varieties of polyarylene ether were studied: Schumacher PAE-2 [77] (also known as Lo- $\kappa$ ™ 2000) and Asahi Chemical ALCAP-E [78]. Both materials have very isotropic  $\kappa$ 's of 2.8. See



**Figure 3-3** Structural formula of two polyarylene ethers: (a) Schumacher PAE-2 [76] and (b) Asahi Chemical ALCAP-E [78]. Ar, Ar', and Ar'' are proprietary aromatic groups.

Figure 3-3. Polyarylene ethers are essentially fully polymerized when spin-coated and can be synthesized by a few approaches. One example is oxidative coupling of phenols, which is employed to synthesize ALCAP-E.



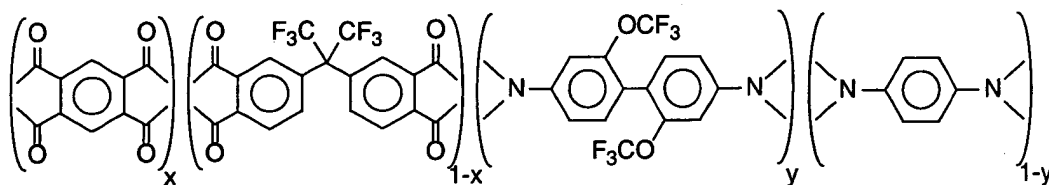
Polyarylene ethers possess many desirable properties for ILD integration but require extensive crosslinking for good thermal stability and solvent resistance. Curing the polymer in oxygen improves crosslinking, but high-temperature exposure to oxygen may not be suitable for Cu integration. Fluorinated polyarylene ether, which exhibit lower  $\kappa$  ( $\kappa = 2.5\text{--}2.6$ ) than nonfluorinated counterparts, has also been synthesized. However, the instability of fluorine in this polymer has resulted in severe metal corrosion, thus rendering integration to be unfeasible.

### 3.3.2 Aromatic Hydrocarbon

SiLK™ polymer, an aromatic hydrocarbon capable of withstanding temperatures in excess of 500°C, was recently developed by Dow Chemical [79]. Since the chemistry of this polymer is yet to be disclosed, SiLK™ polymer will be generically classified as an aromatic hydrocarbon. This material is an isotropic thermoset resin that becomes highly crosslinked in all dimensions upon curing. Although integration of SiLK™ polymer is very sensitive to processing conditions (e.g., cannot withstand exposure to oxygen at high temperatures) [80], the material is under strong consideration by many companies.

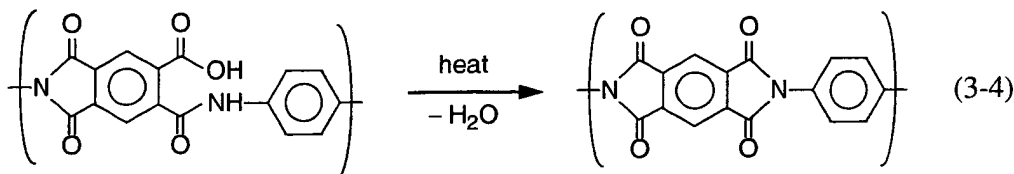
### 3.3.3 Fluorinated Polyimide

Although conventional polyimides do not meet the  $\kappa$  requirements of future ILD's, fluorinated polyimides are potentially suitable candidates [81], [82]. The specific example that was studied is a copolymer called DuPont FPI-136M (Figure 3-4).



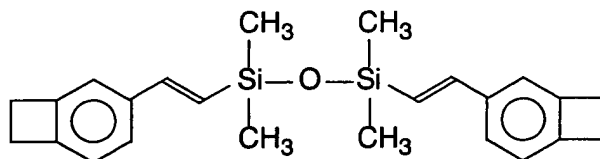
**Figure 3-4** Structural formula of DuPont FPI-136M fluorinated polyimide [82].

Fluorinated polyimide exhibits lower  $\kappa$ , lower moisture uptake, and better isotropy than conventional counterparts. Like other linear polyimides, FPI-136M is formed by cyclization of polyamic acid precursors in the curing step after spin-on deposition. A simplified cyclization reaction is illustrated below.



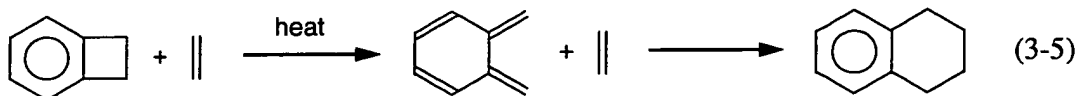
### 3.3.4 Benzocyclobutene

Divinylsiloxane-benzocyclobutene (DVS-BCB), commonly known as benzocyclobutene (BCB), is a thermoset resin derivative of cyclobutane deliberately designed to crosslink when heated [83]. The BCB monomer is shown in Figure 3-5.



**Figure 3-5** Structural formula of Dow Chemical Cyclotene™ 5021 benzocyclobutene (BCB) monomer [83].

Polymerization occurs during the cure step following spin-on deposition. The BCB monomer undergoes a ring opening reaction to give a diene that will react with a C=C to finally give a cyclohexane ring fused to a benzene. Since the BCB monomer has four active sites (two C=C and two cyclobutane rings) for this reaction to occur, the monomer will crosslink into a three-dimensional network, resulting in an isotropic  $\kappa$  of 2.7.

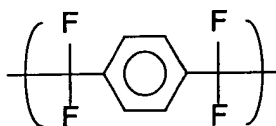


The crosslinking of BCB does not liberate any by-products although the cure must be performed in a non-oxidizing ambient. Otherwise, the polymer will degrade as carbonyl groups (C=O) form. BCB possesses other attractive qualities, such as hydrophobicity, that makes it an attractive and processable low- $\kappa$  ILD. In fact, Damascene Cu integration with BCB has been demonstrated [84]. Unfortunately, the main drawback of BCB is its limited thermal stability. BCB is stable up to only 350°C and is consequently incompatible with many existing backend processes.

A similar derivative of cyclobutane, also developed by Dow Chemical, is perfluorocyclobutane (PFCB) with  $\kappa = 2.4$ . However, similar to other dielectrics having fluorine content, the adhesion of PFCB to common backend films is poor.

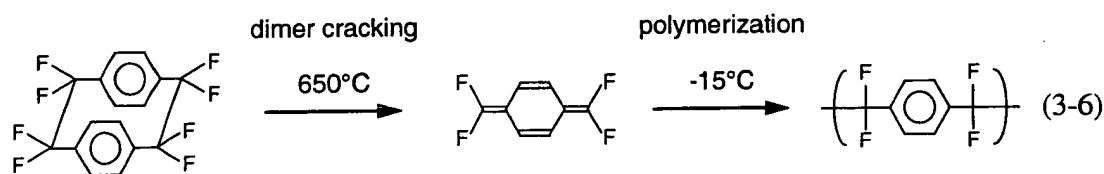
### 3.3.5 Parylene-F

Poly(tetrafluoro-*p*-xylylene) or parylene-F is a vapor-deposited crystalline polymer with  $\kappa$  of 2.3–2.4 [85]. See Figure 3-6.



**Figure 3-6** Structural formula of Novellus AF-4 parylene-F [85].

Dielectric deposition occurs via a sequence of steps [71]. The process involves first the vaporization (or sublimation) of the di-tetrafluoro-*p*-xylylene dimer at about 150°C. The dimer is led into a reactor where it is cracked, or cleaved, at 650°C to form two reactive tetrafluoro-*p*-xylylene monomers. The monomers are led to a vacuum chamber, condense on the wafer surface which is maintained at -15°C, diffuse into the bulk of the parylene-F film, and then polymerize by reacting with the ends of the free-radical polymer chains. The deposition process is surface-reaction-limited. Therefore, the deposition rate can be dramatically increased by lowering the substrate temperature and increasing the surface absorption rate. After deposition, the film must undergo a vacuum anneal at 350°C to stabilize its properties.



Because parylene-F is deposited from the vapor phase, good conformality can be achieved. Parylene-F has been successfully integrated with conventional Al and W metalization. It is yet to be demonstrated in a Damascene Cu scheme where good gapfill ability is not important. The feasibility of parylene-F for Cu integration is questionable considering the thermal, mechanical, adhesion and dimer cost issues associated with this material.

### **3.4 Summary**

This chapter reviewed basic properties of low- $\kappa$  dielectrics and surveyed the families of low- $\kappa$  dielectrics currently evaluated by the industry. The syntheses and chemistries of the six low- $\kappa$  dielectrics investigated in this thesis were described. This chapter and the previous chapter presented the prerequisite information for comprehending specific process integration issues of Cu and low- $\kappa$  polymers—the subjects of the following three chapters. Electrical leakage and anisotropy of fluorinated polyimide are examined in Chapters 4 and 5 respectively while the Cu drift behaviors of the six low- $\kappa$  polymers of Section 3.3 are evaluated in Chapter 6.



**Europäisches  
Patentamt**

**European  
Patent Office**

**Office européen  
des brevets**

# Urkunde Certificate Certificat

Es wird hiermit bescheinigt, daß für die in der beigefügten Patentschrift beschriebene Erfindung ein europäisches Patent für die in der Patentschrift bezeichneten Vertragsstaaten erteilt worden ist.

It is hereby certified that a European patent has been granted in respect of the invention described in the annexed patent specification for the Contracting States designated in the specification.

Il est certifié qu'un brevet européen a été délivré pour l'invention décrite dans le fascicule de brevet ci-joint, pour les Etats contractants désignés dans le fascicule de brevet.

**Europäisches Patent Nr.**

**European Patent No.**

**Brevet européen n°**

**1377990**

**Patentinhaber**

**Proprietor of the Patent**

**Titulaire du brevet**

Vishay Dale Electronics, Inc.  
1122 23rd Street,  
P.O. Box 609  
Columbus,  
Nebraska 68602-0609/US

*Heinrich*

**EXHIBIT**

*2*

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

**EP 1 377 990 B1**

(12)

## EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention  
of the grant of the patent:  
**13.07.2005 Bulletin 2005/28**

(51) Int Cl.7: **H01C 17/075, H01C 7/00,  
H01C 17/12**

(21) Application number: **01924989.5**

(86) International application number:  
**PCT/US2001/012034**

(22) Date of filing: **12.04.2001**

(87) International publication number:  
**WO 2002/082474 (17.10.2002 Gazette 2002/42)**

(54) **THIN FILM RESISTOR HAVING TANTALUM PENTOXIDE MOISTURE BARRIER**

**DÜNNSCHICHTWIDERSTAND MIT TANTALPENTOXID FEUCHTIGKEITSBARRIERE**

**RESISTANCE A COUCHE MINCE COMPRENANT UNE BARRIERE DE PENTOXYDE DE TANTALE  
CONTRE L'HUMIDITE**

(84) Designated Contracting States:  
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE TR**  
Designated Extension States:  
**AL LT LV MK RO SI**

(30) Priority: **09.04.2001 US 829169**

(43) Date of publication of application:  
**07.01.2004 Bulletin 2004/02**

(73) Proprietor: **Vishay Dale Electronics, Inc.  
Columbus, Nebraska 68602-0609 (US)**

(72) Inventor: **VINCENT, Stephen C.  
Columbus, NE 68602 (US)**

(74) Representative: **Wood, Graham  
Bailey Walsh & Co,  
5 York Place  
Leeds LS1 2SD (GB)**

(56) References cited:  
**GB-A- 1 022 075 US-A- 4 161 431  
US-A- 4 837 550**

- **PATENT ABSTRACTS OF JAPAN** vol. 008, no. 120 (M-300), 6 June 1984 (1984-06-06) & JP 59 026277 A (RICOH KK), 10 February 1984 (1984-02-10)
- **PATENT ABSTRACTS OF JAPAN** vol. 013, no. 380 (M-863), 23 August 1989 (1989-08-23) & JP 01 133755 A (SEIKO INSTR & ELECTRON LTD), 25 May 1989 (1989-05-25)
- **PATENT ABSTRACTS OF JAPAN** vol. 014, no. 073 (E-0887), 9 February 1990 (1990-02-09) & JP 01 291401 A (FUJI ELELCTROCHEM CO LTD), 24 November 1989 (1989-11-24)
- **PATENT ABSTRACTS OF JAPAN** vol. 1995, no. 09, 31 October 1995 (1995-10-31) & JP 07 153603 A (HITACHI KOKI CO LTD), 16 June 1995 (1995-06-16)
- **PATENT ABSTRACTS OF JAPAN** vol. 004, no. 086 (P-016), 20 June 1980 (1980-06-20) & JP 55 050221 A (TOKUDA SEISAKUSHO LTD), 11 April 1980 (1980-04-11)

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art

1 377 990 B1

## Description

### BACKGROUND OF THE INVENTION

[0001] This invention relates to a method for a thin film resistor having a tantalum pentoxide moisture barrier.

[0002] Current film resistors and the associated processes of making such resistors have had problems with the ability to create or use an effective moisture barrier. A moisture barrier is that layer that is deposited on the surface of the resistor in order to prevent moisture in the form of condensation or vapor from degrading the resistive film element. Screen-printed material has been used as a moisture barrier and this has been shown to reduce the failure rate of the resistor due to moisture. However, problems remain.

[0003] Tantalum pentoxide has been used in the semiconductor industry as an insulator and to improve recording performance of cobalt alloy media on glass-ceramic disks. Tantalum pentoxide has been used within the resistor industry to improve resistive elements integrated with spark plugs and to form a graze resistor. It is also associated with a tantalum nitride resistive system that prevents moisture failure. It is recognized that tantalum nitride resistors have a naturally occurring layer of tantalum pentoxide, the result of an oxidation process. Further, tantalum nitride resistors and tantalum nitride capacitors are known for their resistance to moisture.

[0004] The document JP 01 291 401 A describes a method of manufacturing a thin film resistor by depositing on a substrate a Ta<sub>2</sub>N film, a Ta film which is then oxidized to form a tantalum pentoxide film.

[0005] Tantalum pentoxide has also been used in thermal heads where a glazed layer is placed on a substrate and a resistor layer is placed on the glazed layer. Japanese publication JP 01 133 755 A discloses such a thermal head with a glazed layer insulating the resistor layer and a protective film such as tantalum pentoxide sputtered onto the resistive layer. A thermal head has a different structure and purpose than a chip resistor. In addition, the chip resistor of the present invention would not include such a glaze layer.

[0006] Many thin film resistors, especially those of nickel-chromium alloys and other alloys containing nickel, chromium, and other metals are particularly susceptible to moisture conditions. These and other types of alloys have a failure mode of electrolytic corrosion that is capable of causing an electrical open under certain moisture conditions. In particular, under powered moisture conditions, electrolytic corrosion can occur and the resistor can fail. This makes the thin film resistor unsuitable for applications where moisture conditions may occur.

[0007] Thus, it is a primary object of the present invention to provide an improved method for a moisture barrier for film resistors.

[0008] Another object of the present invention is to

provide a method for a film resistor which is less susceptible to powered moisture testing.

[0009] Another object of the present invention is to provide a method for a moisture barrier capable of use with nickel-chromium, alloy thin film resistors.

[0010] Yet another object of the present invention is to provide a method for a moisture barrier for thin film resistors that does not require tantalum nitride.

[0011] Another object of the present invention is to provide a method for a moisture barrier for a thin film resistor replaces screen-printed moisture barriers.

[0012] Yet another object of the present invention is to provide a method for a moisture barrier for a thin film resistor that is compatible with normal manufacturing techniques and materials.

[0013] A further object of the present invention is to provide a method for a moisture barrier for a thin film resistor that can be used with nickel and chromium alloys.

[0014] Yet another object of the present invention is to provide a method for a moisture barrier for a thin film resistor that performs favorably under MIL-STD-202 method 103 testing.

[0015] A further object of the present invention is to provide a method for a moisture barrier for a thin film resistor that performs favorably under MIL-STD-202 method 106 testing.

[0016] Yet another object of the present invention is to a method to reduce or eliminate failures of thin film resistors due to electrolytic corrosion under powered moisture conditions.

[0017] Another object of the present invention is to provide a method for a moisture barrier that may be deposited through sputtering.

[0018] These and other objects, features, or advantages of the present invention will become apparent from the specification and claims.

### BRIEF SUMMARY OF THE INVENTION

[0019] The present invention is a method for manufacturing a thin film chip resistors with a tantalum pentoxide moisture barrier. The invention provides for a tantalum pentoxide moisture barrier to be used in manufacturing a thin film resistor using otherwise standard manufacturing processes. The invention permits any number of metal films to be used as the resistive element. In particular, the invention permits nickel-chromium alloys to be used. The resistive metal film layer is overlaid with a moisture barrier of tantalum pentoxide. The tantalum pentoxide layer acts as a moisture barrier.

[0020] The tantalum pentoxide layer results in a thin film resistor that is resistive to moisture. In particular, the tantalum pentoxide moisture barrier allows the thin film resistor to be more resistant to electrolytic corrosion that causes an electrical open under certain moisture conditions. Thus the present invention provides for increased reliability in thin film resistors while using substantially

conventional manufacturing techniques.

**[0021]** The method of the present invention is defined by the features of claim 1 and comprises depositing a metal film resistive layer directly overlaying and attaching to a thin film chip resistor substrate. The method further comprises attaching a chip resistor termination on each end of the metal film resistive layer. A moisture barrier consisting essentially of a layer of tantalum pentoxide film is deposited in an overlying relationship to the metal film resistive layer to reduce failures due to electrolytic corrosion under powered moisture conditions. The layer of tantalum pentoxide is not formed by a natural oxidation of the metal thin film resistive layer.

**[0022]** The resistor of the present invention is defined by the features of claims 8 or 13 and is formable according to the above described method. The resistor may include the tantalum pentoxide directly overlying and being attached to the resistive element or a passivation layer may be interposed between the moisture barrier and the film resistive layer.

#### BRIEF DESCRIPTION OF THE DRAWINGS

##### **[0023]**

Figure 1 is a side view of a prior art thin film resistor. Figure 2 is a side view of the thin film resistor having a tantalum pentoxide moisture barrier of the present invention.

Figure 3 is a flow chart showing a method of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0024]** Figure 1 shows a prior art thin film resistor that may be manufactured with standard manufacturing processes. In Figure 1, a substrate 12 is used. The substrate 12 may be alumina or other substrate that may be used in thin film processes. Overlaid on the substrate is a layer of a metal film which serves as the resistive element for the thin film resistor. The metal film layer 14 may be any number of metal films but is often a nickel-chromium (nichrome) alloy or other alloy containing nickel and/or chromium. Nickel-chromium is one of the most common types of metal films used in thin film resistors. Overlaying the metal film layer 14 is passivation layer 16. The passivation layer 16 may be used to protect the thin film resistors electronic properties from deterioration from external contaminants. The passivation layer 16 may be a deposited scratch resistant material such as silicon nitride, silicon dioxide, or other materials such as may be known in the art. The thin film resistor 10 also includes termination 18. The termination 18 on the ends of the thin film resistor is used to electrically connect the thin film resistor.

**[0025]** The thin film resistor of the present invention is shown in Figure 2. The thin film resistor 20 is manufactured in a manner similar to the thin film resistor 10

of Figure 1. However, the thin film resistor 20 of Figure 2 also includes a moisture barrier layer 22. The moisture barrier layer 22 is a layer of tantalum pentoxide film. The tantalum pentoxide film may be sputtered onto the thin film resistor, the tantalum pentoxide layer overlaying the resistive metal film layer and optionally a passivation layer. The present invention contemplates that the passivation layer need not be used.

**[0026]** The addition of the tantalum pentoxide layer reduces failure due to electrolytic corrosion that causes an electrical open under certain moisture conditions. The thin film resistor 20 may use alumina as substrate 12, or other substrate material. The present invention is no way limited to the particular selection of the substrate, however, the present invention is capable of use in standard manufacturing processes. The passivation layer may be a layer of silicon nitride, silicon dioxide, or other material such as may be known in the art. The present invention contemplates that any number of metal films could be used, including metal films containing nickel, chromium, or both. Termination 18 for the thin film resistor 20 may be any type of termination typically used with thin film resistors. For example, termination 18 may include wrap around termination.

**[0027]** The thin film resistor of the present invention using a nickel-chromium metal film layer and having a tantalum pentoxide moisture barrier has been evaluated according to standard environmental test methods. The thin film resistor using a 1206-size wrap around termination chip resistor subjected to MIL-STD-202 method 103 tests. These tests are designed to evaluate the properties of materials used in electronic components as they are influenced by the absorption and defusion of moisture and moisture vapor. The test is an accelerated environmental test that uses high relative humidity and an elevated temperature. According to the test a temperature of 40°C and a relative humidity of between 90% and 95% was used. 10 Volts DC was applied to the resistors for 96 hours.

**[0028]** In the 96-hour test, the typical failure rate (without tantalum pentoxide) is from 0 to 4 parts per lot test open. Testing of the tantalum pentoxide moisture barrier thin film resistors where tantalum pentoxide was used as a moisture barrier indicates that there were no opens.

**[0029]** A second test was conducted with a second group of thin film resistors having the tantalum pentoxide moisture barrier. For the second test, the MIL-STD-202 method 106 was used for testing moisture resistance. This test differs from the previous test as it uses temperature cycling to provide alternate periods of condensation and drying. According to this test, the temperature range selected was between 65°C to -10°C with a relative humidity of between 90% and 100%. The test was conducted over a 240 hour period with 10 Volts DC applied.

**[0030]** In typical results for the 240 hour test (no tantalum pentoxide moisture barrier), approximately 90 percent of the resistors test fail. Test results for the 240

hour test where tantalum pentoxide is used as a moisture barrier reveal that there were no failures.

**[0031]** The method of manufacturing the thin film resistor of the present invention is best shown in Figure 3. The thin film resistor of the present invention can be manufactured in a manner substantially consistent with thin film manufacturing processes. In step 30 a metal film is deposited through sputtering or other techniques. The metal film may be of an alloy containing copper, chromium, nichrome, or other metal such as may be known in the art. Optionally, in step 32, a passivation layer is deposited. The passivation layer is deposited through sputtering or through other techniques. The passivation layer is used to protect the thin film resistor from external contaminants. In step 34, a layer of tantalum pentoxide is deposited. The tantalum pentoxide layer may be deposited through sputtering or other techniques. The tantalum pentoxide layer serves as a moisture barrier to reduce electrolytic corrosion of the thin film resistor.

**[0032]** Thus, an apparatus and method for a thin film resistor having a tantalum pentoxide moisture barrier has been disclosed which solves problems and deficiencies in the art.

#### Claims

1. A method of manufacturing a thin film chip resistor with a moisture barrier comprising: depositing a metal film resistive layer directly overlaying and attaching to a thin film chip resistor substrate; attaching a chip resistor termination on each end of the metal film resistive layer; and depositing the moisture barrier consisting essentially of a layer of tantalum pentoxide film overlaying the metal film resistive layer to reduce failures due to electrolytic corrosion under powered moisture conditions, the layer of tantalum pentoxide not being formed by natural oxidation of the metal thin film resistive layer.
2. The method according to claim 1 and further comprising directly overlaying and attaching the moisture barrier to the film resistive layer.
3. The method according to claim 1 and further comprising directly overlaying and attaching a passivation layer to the metal film resistive layer and directly overlaying and attaching the moisture barrier to the passivation layer.
4. The method of claim 1 wherein the step of depositing a layer of tantalum pentoxide is sputtering tantalum pentoxide film.
5. The method of claim 1 wherein the metal film layer is an alloy containing nickel.
6. The method of claim 1 wherein the metal film layer is an alloy containing chromium.
7. The method of claim 1 wherein the metal film layer is a nickel-chromium alloy.
8. A thin film chip resistor (20) manufacturable by the method according to claim 1 comprising: a substrate (12); a metal thin film resistive layer (14) directly attached to the substrate, a chip resistor termination (18) attached on each end of the metal thin film resistive layer (14); and an outer moisture barrier (22) consisting essentially of tantalum pentoxide directly overlaying and attaching to the metal thin film resistive layer (14) for reducing failures due to electrolytic corrosion under powered moisture conditions, the tantalum pentoxide not being formed by natural oxidation of the metal thin film resistive layer.
9. The thin film chip resistor (20) of claim 8 wherein the metal thin film resistive layer (14) is an alloy containing nickel.
10. The thin film chip resistor (20) of claim 8 wherein the metal thin film resistive layer (14) is an alloy containing chromium.
11. The thin film chip resistor (20) of claim 8 wherein the metal thin film resistive layer (14) is a nickel-chromium alloy.
12. The thin film chip resistor (20) of claim 8 wherein the tantalum pentoxide is overlaid by sputtering.
13. A thin film chip resistor (20) manufacturable according to the method of claim 1 comprising: a resistive substrate (12); a metal thin film resistive layer (14) directly attached to the substrate (12), the metal thin film being non-tantalum; a chip resistor termination (18) attached on each end of the metal thin film resistive layer (14); a passivation layer (16) directly overlaying the metal thin film resistive layer (14); an outer moisture barrier (22) consisting of tantalum pentoxide directly overlaying the passivation layer (16) for reducing failures due to electrolytic corrosion under powered moisture conditions, the tantalum pentoxide layer not being formed naturally by oxidation.

#### Patentansprüche

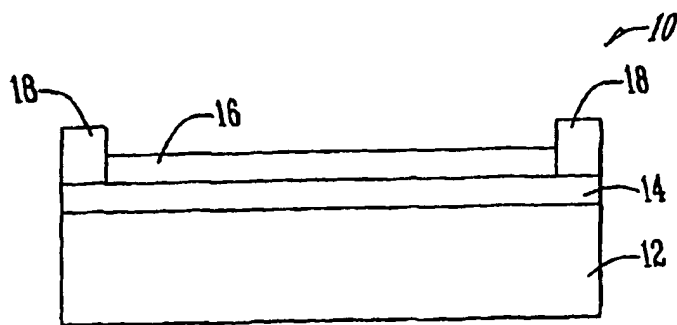
1. Verfahren zur Herstellung eines Dünnschicht-Chipwiderstands mit einer Feuchtigkeitsbarriere, umfassend die folgenden Schritte: Auftragen einer ohmschen Metallfoliensicht direkt auf ein Dünnschicht-Chipwiderstandssubstrat und Befestigen

- derselben daran; Anbringen eines Chipwiderstandsabschlusses an jedem Ende der ohmschen Metallfolienschiicht; und Auftragen der Feuchtigkeitsbarriere, die im Wesentlichen aus einer Tantalpentoxidfolienschiicht besteht, die auf der ohmschen Metallfolienschiicht liegt, um Ausfälle aufgrund von elektrolytischer Korrosion bei Stromzufuhr unter feuchten Bedingungen zu reduzieren, wobei die Tantalpentoxidschiicht nicht durch natürliche Oxidation der ohmschen dünnen Metallfolienschiicht entsteht.
2. Verfahren nach Anspruch 1, ferner umfassend das direkte Legen der Feuchtigkeitsbarriere auf die ohmsche Folienschicht und das Befestigen daran.
  3. Verfahren nach Anspruch 1, ferner umfassend das direkte Legen einer Passivierungsschiicht auf die ohmsche Metallfolienschiicht und das Befestigen daran und das direkte Auflegen der Feuchtigkeitsbarriere auf die Passivierungsschiicht und das Befestigen daran.
  4. Verfahren nach Anspruch 1, wobei der Schritt des Auftragens einer Schicht aus Tantalpentoxid das Aufstäuben einer Tantalpentoxidschiicht ist.
  5. Verfahren nach Anspruch 1, wobei die Metallfolienschiicht eine nickelhaltige Legierung ist.
  6. Verfahren nach Anspruch 1, wobei die Metallfolienschiicht eine chromhaltige Legierung ist.
  7. Verfahren nach Anspruch 1, wobei die Metallfolienschiicht eine Nickel-Chrom-Legierung ist.
  8. Dünnschiicht-Chipwiderstand (20), der mit dem Verfahren nach Anspruch 1 hergestellt werden kann und Folgendes umfasst: ein Substrat (12); eine ohmsche dünne Metallfolienschiicht (14), die direkt auf dem Substrat befestigt wird, einen Chipwiderstandsabschluss (18), der an jedem Ende der ohmschen dünnen Metallfolienschiicht (14) befestigt wird; und eine äußere Feuchtigkeitsbarriere (22), die im Wesentlichen aus Tantalpentoxid besteht, das direkt auf die ohmsche dünne Metallfolienschiicht (14) aufgebracht und daran befestigt wird, um Ausfälle aufgrund von elektrolytischer Korrosion bei Stromzufuhr unter feuchten Bedingungen zu reduzieren, wobei das Tantalpentoxid nicht durch natürliche Oxidation der ohmschen dünnen Metallfolienschiicht gebildet wird.
  9. Dünnschiicht-Chipwiderstand (20) nach Anspruch 8, wobei die ohmsche dünne Metallfolienschiicht (14) eine nickelhaltige Legierung ist.
  10. Dünnschiicht-Chipwiderstand (20) nach Anspruch 8, wobei die ohmsche dünne Metallfolienschiicht (14) eine chromhaltige Legierung ist.
  11. Dünnschiicht-Chipwiderstand (20) nach Anspruch 8, wobei die ohmsche dünne Metallfolienschiicht (14) eine Nickel-Chrom-Legierung ist.
  12. Dünnschiicht-Chipwiderstand (20) nach Anspruch 8, wobei das Tantalpentoxid durch Aufstäuben aufgelegt wird.
  13. Dünnschiicht-Chipwiderstand (20), der mit dem Verfahren nach Anspruch 1 hergestellt werden kann und Folgendes umfasst: ein ohmsches Substrat (12); eine ohmsche dünne Metallfolienschiicht (14), die direkt an dem Substrat (12) befestigt wird, wobei die dünne Metallschiicht kein Tantal ist; einen Chipwiderstandsabschluss (18), der an jedem Ende der ohmschen dünnen Metallfolienschiicht (14) befestigt wird; eine Passivierungsschiicht (16), die direkt auf der ohmschen dünnen Metallfolienschiicht (14) liegt; eine äußere Feuchtigkeitsbarriere (22), die aus Tantalpentoxid besteht, das direkt auf der Passivierungsschiicht (16) liegt, um Ausfälle aufgrund von elektrolytischer Korrosion bei Stromzufuhr unter feuchten Bedingungen zu reduzieren, wobei die Tantalpentoxidschiicht nicht natürlich durch Oxidation gebildet wird.

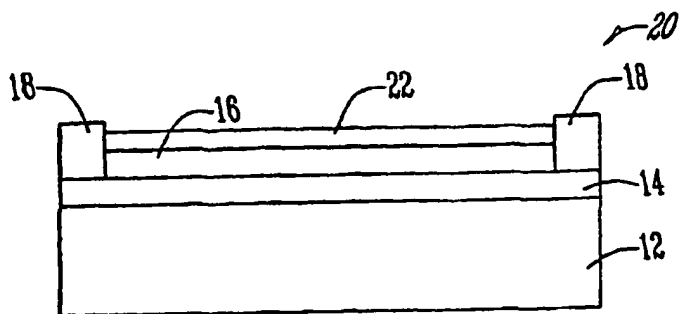
#### Revendications

1. Procédé de fabrication d'une résistance pastille à couche mince avec une barrière de pentoxyde de tantale contre l'humidité, comprenant : le dépôt d'une couche résistive à pellicule métallique qui est superposée directement à un substrat de résistance pastille à couche mince et s'y attache ; la fixation d'une terminaison de résistance pastille sur chaque extrémité de la couche résistive à pellicule métallique ; et le dépôt de la barrière contre l'humidité, qui se compose essentiellement d'une couche à pellicule de pentoxyde de tantale et qui recouvre la couche résistive à pellicule métallique dans le but de réduire les défaillances dues à la corrosion électrolytique dans des conditions d'humidité sous tension, alors que la couche de pentoxyde de tantale n'est pas formée par une oxydation naturelle de la couche résistive à pellicule métallique mince.
2. Le procédé selon la revendication 1, et comprenant en outre l'action consistant à superposer directement et à attacher la barrière contre l'humidité à la couche résistive à pellicule.
3. Le procédé selon la revendication 1, et comprenant en outre l'action consistant à superposer directement et à attacher une couche de passivation à la

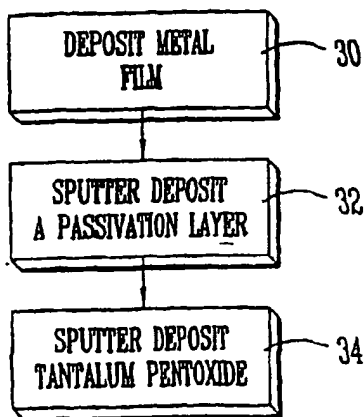
- couche résistive à pellicule métallique ainsi que l'action consistant à superposer directement et à attacher la bamère contre l'humidité à la couche de passivation.
4. Le procédé selon la revendication 1, dans lequel l'étape de dépôt d'une couche de pentoxyde de tantale consiste à pulvériser une pellicule de pentoxyde de tantale.
5. Le procédé selon la revendication 1, dans lequel la couche à pellicule métallique est un alliage contenant du nickel.
6. Le procédé selon la revendication 1, dans lequel la couche à pellicule métallique est un alliage contenant du chrome.
7. Le procédé selon la revendication 1, dans lequel la couche à pellicule métallique est un alliage de nickel-chrome.
8. Résistance pastille (20) à couche mince pouvant être fabriquée par le procédé conforme à la revendication 1 comprenant : un substrat (12) ; une couche résistive à pellicule métallique mince (14) laquelle est directement attachée au substrat, une terminaison (18) de résistance pastille étant attachée sur chaque extrémité de la couche résistive à pellicule métallique mince (14) ; et une barrière externe (22) contre l'humidité essentiellement constituée de pentoxyde de tantale qui est directement superposée à la couche résistive à pellicule métallique mince (14), et qui y est attachée, afin de réduire les défaillances dues à la corrosion électrolytique se produisant sous des conditions d'humidité sous tension, alors que le pentoxyde de tantale n'est pas formé par une oxydation naturelle de la couche résistive à pellicule métallique mince.
9. La résistance pastille (20) à couche mince de la revendication 8, dans laquelle la couche résistive à pellicule métallique mince (14) est un alliage contenant du nickel.
10. La résistance pastille (20) à couche mince de la revendication 8, dans laquelle la couche résistive à pellicule métallique mince (14) est un alliage contenant du chrome.
11. La résistance pastille (20) à couche mince de la revendication 8, dans laquelle la couche résistive à pellicule métallique mince (14) est un alliage contenant du nickel-chrome.
12. La résistance pastille (20) à couche mince de la revendication 8, dans laquelle le pentoxyde de tantale est superposé par pulvérisation.
13. Résistance pastille (20) à couche mince pouvant être fabriquée conformément au procédé de la revendication 1 comprenant : un substrat résistif (12) ; une couche résistive à pellicule métallique mince (14) laquelle est directement attachée au substrat (12), la pellicule métallique mince n'étant pas du tantale ; une terminaison (18) de résistance pastille, laquelle est attachée sur chaque extrémité de la couche résistive à pellicule métallique mince (14) ; une couche de passivation (16), laquelle est directement superposée à la couche résistive à pellicule métallique mince (14) ; une barrière externe (22) contre l'humidité constituée de pentoxyde de tantale qui est directement superposée à la couche de passivation (16) afin de réduire les défaillances dues à la corrosion électrolytique se produisant sous des conditions d'humidité sous tension, alors que la couche de pentoxyde de tantale n'est pas formée naturellement par oxydation.



*Fig. 1 (PRIOR ART)*



*Fig. 2*



*Fig. 3*